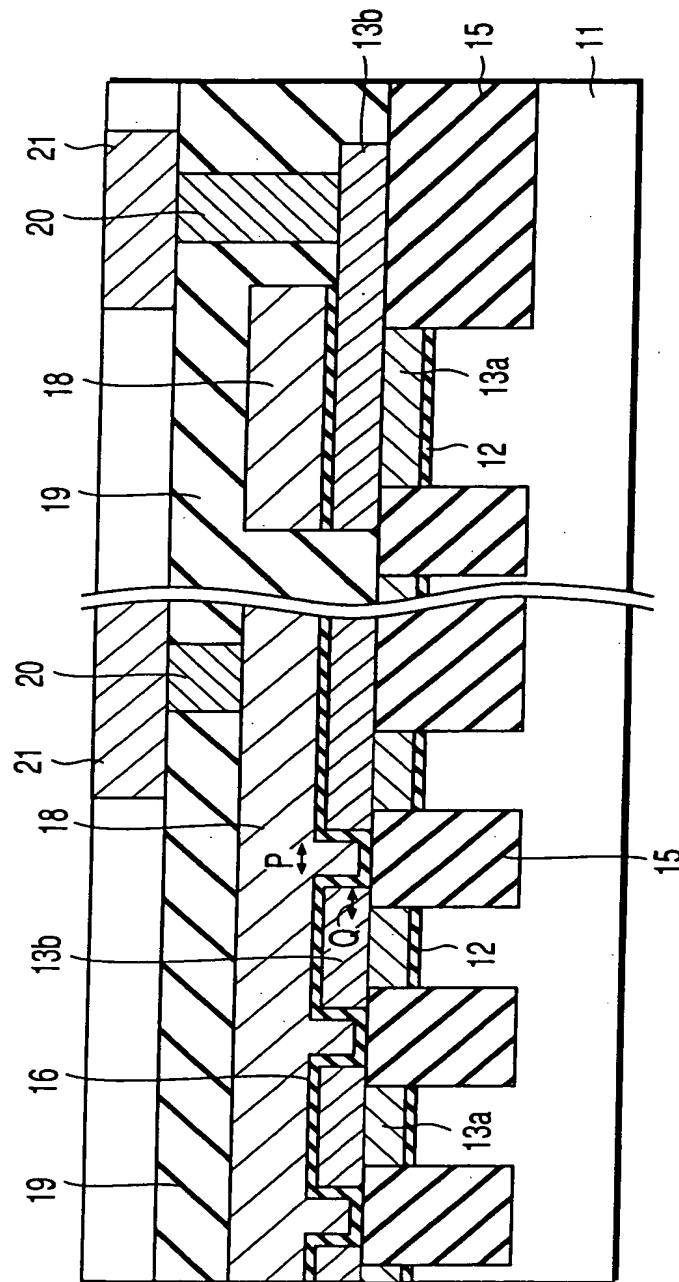


FIG. 46A
RELATED ART

FIG. 46B
RELATED ART

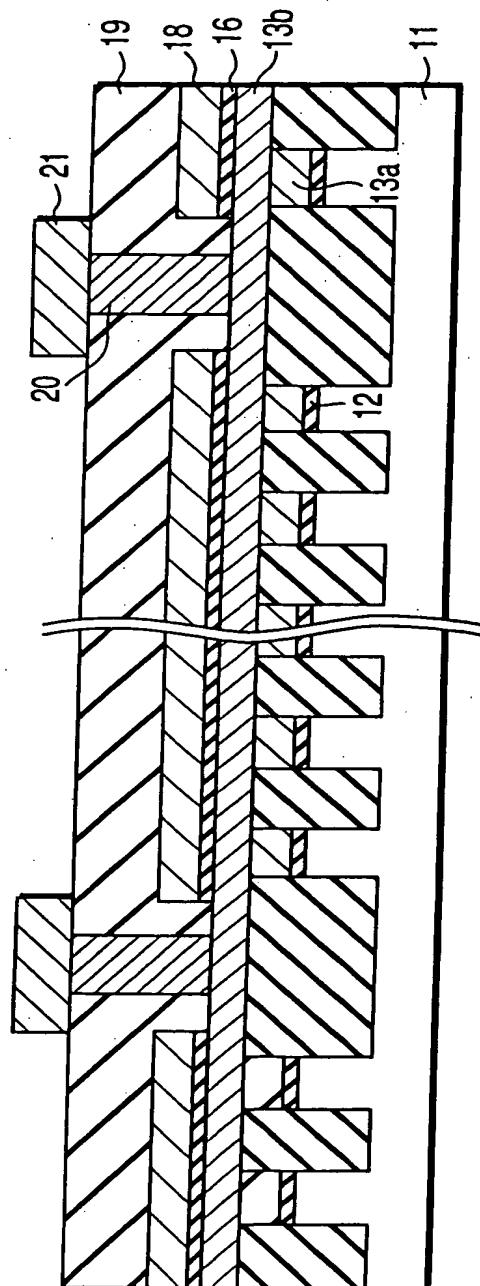


Peripheral circuit region

Memory cell array region

FIG. 47A

RELATED ART



Selective gate region

FIG. 47B
RELATED ART

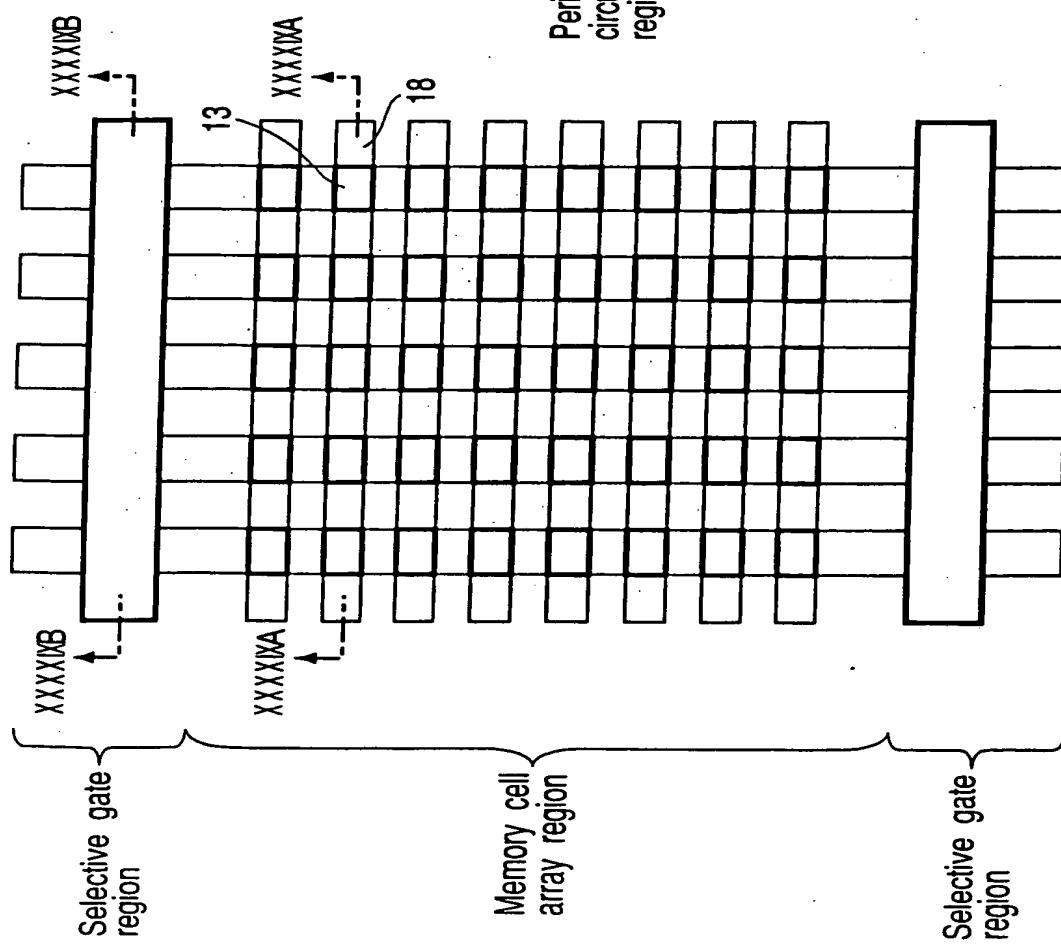


FIG. 48A
RELATED ART

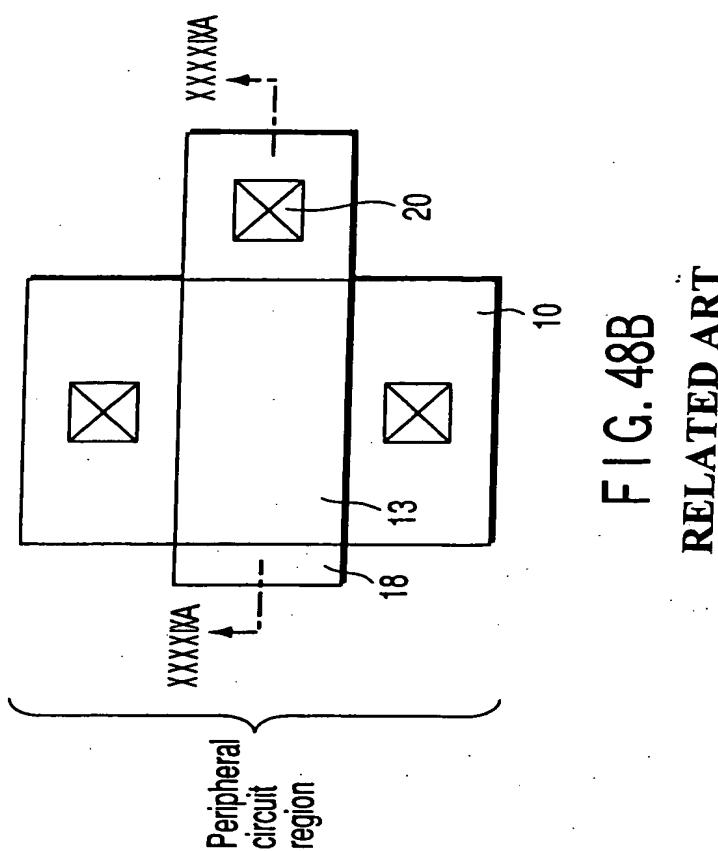


FIG. 48B
RELATED ART

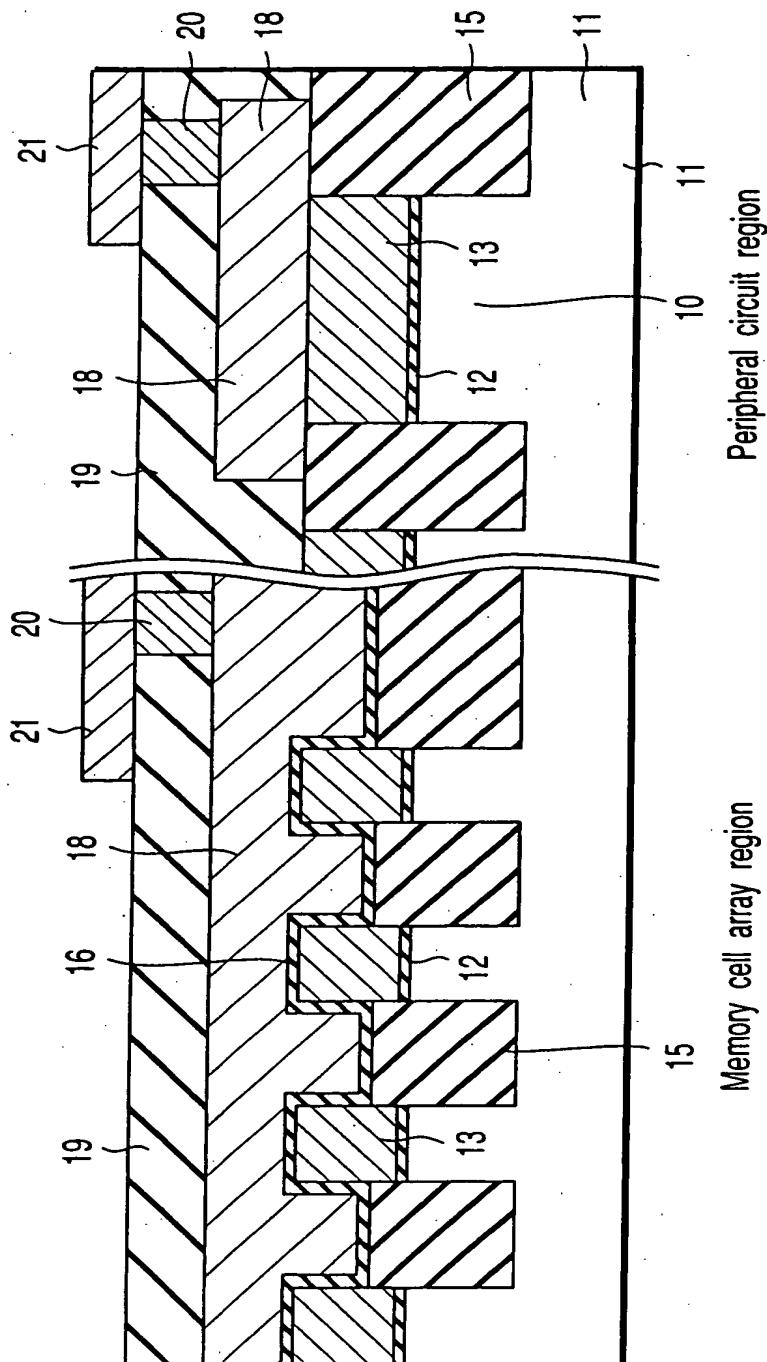
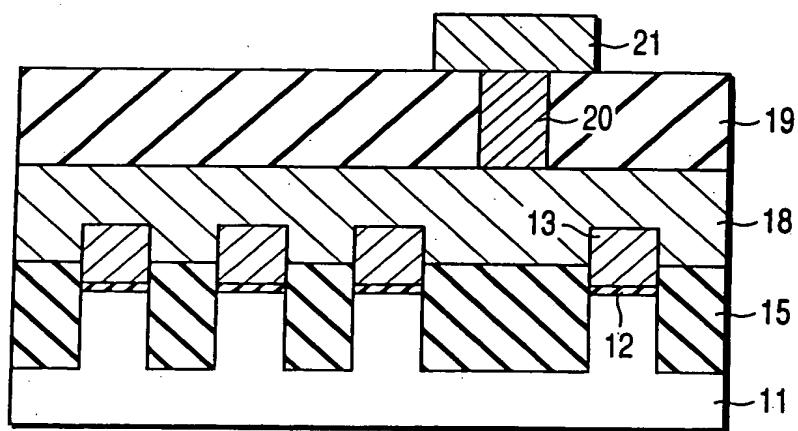


FIG. 49A
RELATED ART



Selective gate region

FIG. 49B
RELATED ART